Lecture 20:
Scheduling the Graphics Pipeline on a GPU

Visual Computing Systems
CMU 15-769, Fall 2016
Today

- Real-time 3D graphics workload metrics
- Scheduling the graphics pipeline on a modern GPU
Quick aside: tessellation
Triangle size
(data from 2010)

Percentage of total triangles

Triangle area (pixels)

[source: NVIDIA]
Low geometric detail

Credit: Pro Evolution Soccer 2010 (Konami)
Surface tessellation

Procedurally generate fine triangle mesh from coarse mesh representation
Graphics pipeline with tessellation

Five programmable stages in modern pipeline (OpenGL 4, Direct3D 11)

- **Vertices**: 1 in / 1 out
- **Primitives**: 3 in / 1 out (for tris), 1 in / small N out
- **Fragments**: 1 in / N out
- **Pixels**: 1 in / 0 or 1 out

**Vertex Generation**
- **Coarse Vertices**: 1 in / 1 out
- **Tessellation**
- **Fine Vertices**: 1 in / 1 out

**Primitive Generation**
- **Coarse Primitives**: 1 in / 1 out
- **Fine Primitives**: 3 in / 1 out (for tris), 1 in / small N out

**Rasterization**
- **Rasterization (Fragment Generation)**
- **Fragments**: 1 in / N out

**Fragment Processing**
- **Fine Primitives**: 1 in / small N out
- **Fragment Processing**
- **Frames**: 1 in / 0 or 1 out

**Frame-Buffer Ops**
Graphics workload metrics
Key 3D graphics workload metrics

- Data amplification from stage to stage
  - Triangle size (amplification in rasterizer)
  - Expansion during primitive processing (if enabled)
  - Tessellation factor (if tessellation enabled)

- [Vertex/fragment/geometry] shader cost
  - How many instructions?
  - Ratio of math to data access instructions?

- Scene depth complexity
  - Determines number of depth and color buffer writes
  - Recall: early/high Z-cull optimizations are most efficient when pipeline receives triangles in depth order
Amount of data generated (size of stream between consecutive stages)

Compact geometric model

High-resolution (post tessellation) mesh

“Diamond” structure of graphics workload

Intermediate data streams tend to be larger than scene inputs or image output

Frame buffer pixels

Fine Primitive Generation
- Coarse Vertices: 1 in / 1 out
  - Vertex Processing
  - Coarse Primitives: 1 in / 1 out
  - Tessellation
  - Fine Vertices: 1 in / 1 out
  - Fine Primitive Generation
  - Fine Primitives: 1 in / small N out
    - Fine Primitive Processing
    - Rasterization (Fragment Generation)
    - Fragments: 1 in / N out
      - Fragment Processing
      - Pixels: 1 in / 0 or 1 out
        - Frame-Buffer Ops
Scene depth complexity

Rough approximation: \( TA = SD \)

\( T \) = # triangles
\( A \) = average triangle area
\( S \) = pixels on screen
\( D \) = average depth complexity
Graphics pipeline workload changes dramatically across draw commands

- Triangle size is scene and frame dependent
  - Move far away from an object, triangles get smaller
  - Vary within a frame (characters are usually higher resolution meshes)

- Varying complexity of materials, different number of lights illuminating surfaces
  - No such thing as an “average” shader
  - Tens to several hundreds of instructions per shader

- Stages can be disabled
  - Shadow map creation = NULL fragment shader
  - Post-processing effects = no vertex work

- Thousands of state changes and draw calls per frame

Example: rendering a “depth map” requires vertex shading but no fragment shading
Parallelizing the graphics pipeline

Adopted from slides by Kurt Akeley and Pat Hanrahan (Stanford CS448 Spring 2007)
We're now going to talk about this scheduler.
Reminder: requirements + workload challenges

- Immediate mode interface: pipeline accepts sequence of commands
  - Draw commands
  - State modification commands

- Processing commands has sequential semantics
  - Effects of command A must be visible before those of command B

- Relative cost of pipeline stages changes frequently and unpredictably
  (e.g., due to changing triangle size, rendering mode)

- Ample opportunities for parallelism
  - Many triangles, vertices, fragments, etc.
Simplified pipeline

For now: just consider all geometry processing work (vertex/primitive processing, tessellation, etc.) as "geometry" processing.

(I’m drawing the pipeline this way to match tonight’s readings)
Simple parallelization (pipeline parallelism)

Separate hardware unit is responsible for executing work in each stage

What is my maximum speedup?
A cartoon GPU:
Assume we have four separate processing pipelines
Leverages data-parallelism present in rendering computation
Molnar’s sorting taxonomy

Implementations characterized by where communication occurs in pipeline

Sort first
- Geometry Processing

Sort middle
- Rasterization

Sort last fragment
- Fragment Processing

Sort last image composition
- Frame-Buffer Ops

Note: The term “sort” can be misleading for some. It may be helpful to instead consider the term “distribution” rather than sort. The implementations are characterized by how and when they redistribute work onto processors.

* The origin of the term sort was from “A Characterization of Ten Hidden-Surface Algorithms”. Sutherland et al. 1974
Sort first
Assign each replicated pipeline responsibility for a region of the output image
Do minimal amount of work (compute screen-space vertex positions of triangle) to determine which region(s) each input primitive overlaps
Sort first work partitioning
(partition the primitives to parallel units based on screen overlap)

1

2

3

4
Sort first

- **Good:**
  - Simple parallelization: just replicate rendering pipeline and operate independently (order maintained in each)
  - More parallelism = more performance
  - Small amount of sync/communication (communicate original triangles)
  - Early fine occlusion cull ("early z") just as easy as single pipeline

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**Application**

- Geometry Processing
  - Rasterization
  - Fragment Processing
  - Frame-Buffer Ops

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**Output image**
Bad:
- Potential for workload imbalance (one part of screen contains most of scene)
- Extra cost of triangle “pre-transformation” (needed to sort)
- “Tile spread”: as screen tiles get smaller, primitives cover more tiles (duplicate geometry processing across multiple parallel pipelines)
Sort first examples

- **WireGL/Chromium** (parallel rendering with a cluster of GPUs)
  - "Front-end" sorts primitives to machines
  - Each GPU is a full rendering pipeline (responsible for part of screen)

- Pixar’s RenderMan
  - Multi-core software renderer
  - Sort surfaces into tiles prior to tessellation

*Chromium can also be configured as a sort-last image composition system*
Sort middle
Sort middle

Distribute primitives to pipelines (e.g., round-robin distribution)

**Assign each rasterizer a region of the render target**

Sort after geometry processing based on screen space projection of primitive vertices
Interleaved mapping of screen

- Decrease chance of one rasterizer processing most of scene
- Most triangles overlap multiple screen regions (often overlap all)
Fragment interleaving in NVIDIA Fermi

Fine granularity interleaving

Coarse granularity interleaving

Question 1: what are the benefits/weaknesses of each interleaving?

Question 2: notice anything interesting about these patterns?
Sort middle interleaved

- Good:
  - Workload balance: both for geometry work AND onto rasterizers (due to interleaving)
  - Does not duplicate geometry processing for each overlapped screen region
Sort middle interleaved

- **Bad:**
  - Bandwidth scaling: sort is implemented as a broadcast (each triangle goes to many/all rasterizers)
  - If tessellation is enabled, must communicate many more primitives than sort first
  - Duplicated per triangle setup work across rasterizers
SGI RealityEngine

Sort-middle interleaved design

[Akeley 93]
# Tiling (a.k.a. “chunking”, “bucketing”)

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>0</th>
<th>1</th>
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</tbody>
</table>

**Interleaved (static) assignment to processors**

<table>
<thead>
<tr>
<th>B0</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>B4</th>
<th>B5</th>
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<td>B8</td>
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<tr>
<td>B12</td>
<td>B13</td>
<td>B14</td>
<td>B15</td>
<td>B16</td>
<td>B17</td>
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<td>B18</td>
<td>B19</td>
<td>B20</td>
<td>B21</td>
<td>B22</td>
<td>B23</td>
</tr>
</tbody>
</table>

**Assignment to buckets**

List of buckets is a work queue. Buckets are dynamically assigned to processors.
**Sort middle tiled (chunked)**

**Phase 1:** Populate buckets with triangles

- Buckets stored in off-chip memory

**Phase 2:** Process buckets (one bucket per processor at a time)

- Rasterization
- Fragment Processing
- Frame-Buffer Ops

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Partition screen into many small tiles (many more tiles than physical rasterizers)
Sort geometry by tile into buckets (one bucket per tile of screen)
After all geometry is bucketed, rasterizers process buckets in parallel
Sort middle tiled (chunked)

- **Good:**
  - Good load balance (distribute many buckets onto rasterizers)
  - Potentially low bandwidth requirements (why? when?)
    - Question: What should the size of tiles be for maximum BW savings?
  - Challenge: “bucketing” sort has low contention (assuming each triangle only touches a small number of buckets), but there still is contention

- **Recent examples:**
  - Many mobile GPUs: Imagination PowerVR, ARM Mali, Qualcomm Adreno
  - Parallel software rasterizers
    - Intel Larrabee software rasterizer
    - NVIDIA CUDA software rasterizer
Sort last
Sort last fragment

Distribute primitives to top of pipelines (e.g., round robin)
Sort after fragment processing based on (x,y) position of fragment
Sort last fragment

- Good:
  - No redundant geometry processing or rasterization (but early z-cull is a problem)
  - Point-to-point communication during sort
  - Interleaved pixel mapping results in good workload balance for frame-buffer ops
Bad:
- Pipelines may stall due to primitives of varying size (due to order requirement)
- Bandwidth scaling: many more fragments than triangles
- Hard to implement early occlusion cull (more bandwidth challenges)
Sort last image composition

Each pipeline renders some fraction of the geometry in the scene. Combine the color buffers, according to depth, into the final image.
Sort last image composition

Z comp

Other combiners possible
Sort last image composition

- Breaks abstraction: cannot maintain pipeline’s sequential semantics

- Simple implementation: N separate rendering pipelines
  - Can use off-the-shelf GPUs to build a massive rendering system
  - Coarse-grained communication (image buffers)

- Similar load imbalance problems as sort-last fragment

- Under high depth complexity, bandwidth requirement is lower than sort last fragment
  - Communicate final pixels, not all fragments
Recall: modern OpenGL 4 / Direct3D 11 pipeline

Five programmable stages
Modern GPU: programmable parts of pipeline virtualized on pool of programmable cores

Hardware is a **heterogeneous** collection of resources (programmable and non-programmable)

Programmable resources are time-shared by vertex/primitive/fragment processing work
Must keep programmable cores busy: sort everywhere
Hardware work distributor assigns work to cores (based on contents of inter-stage queues)
Sort everywhere

(How modern high-end GPUs are scheduled)
Sort everywhere

Distribute primitives to top of pipelines
Redistribute after geometry processing (e.g., round robin)
Sort after fragment processing based on (x, y) position of fragment
Implementing sort everywhere

(Challenge: rebalancing work at multiple places in the graphics pipeline to achieve efficient parallel execution, while maintaining triangle draw order)
Starting state: draw commands enqueued for pipeline

Input: three triangles to draw
(fragments to be generated for each triangle by rasterization are shown below)

Assume batch size is 2 for assignment to rasterizers.
After geometry processing, first two processed triangles assigned to rast 0

Input:

Assume batch size is 2 for assignment to rasterizers.
Assign next triangle to rast 1 (round robin policy, batch size = 2)

Q. What is the ‘next’ token for?

Input:

Draw ▲ T1 → 1 2 3 4
Draw ▲ T2 → 1 2 3 4
Draw ▲ T3 → 1 2 3

Interleaved render target
Rast 0 and rast 1 can process T1 and T3 simultaneously
(Shaded fragments enqueued in frame-buffer unit input queues)
FB 0 and FB 1 can simultaneously process fragments from rast 0
(Notice updates to frame buffer)
Fragments from T3 cannot be processed yet. Why?

Input:

```
Draw T1  →  1  2  3  4
Draw T2  →  1  2  3  4
Draw T3  →  1  2  3
```

Interleaved render target
Rast 0 processes T2
(Shaded fragments enqueued in frame-buffer unit input queues)
Rast 0 broadcasts ‘next’ token to all frame-buffer units

Input:

- Draw ▲₁ → 1 2 3 4
- Draw ▲₂ → 1 2 3 4
- Draw ▲₃ → 1 2 3

Interleaved render target
FB 0 and FB 1 can simultaneously process fragments from rast 0
(Notice updates to frame buffer)

Input:

Draw $\triangledown T_1 \rightarrow 1 \ 2 \ 3 \ 4$
Draw $\triangledown T_2 \rightarrow 1 \ 2 \ 3 \ 4$
Draw $\triangledown T_3 \rightarrow 1 \ 2 \ 3$

Interleaved render target
Switch token reached: frame-buffer units start processing input from rast 1

Input:

Draw \( \text{T1} \) → 
\[ \begin{array}{cccc}
1 & 2 & 3 & 4 \\
\end{array} \]

Draw \( \text{T2} \) → 
\[ \begin{array}{cccc}
1 & 2 & 3 & 4 \\
\end{array} \]

Draw \( \text{T3} \) → 
\[ \begin{array}{ccc}
1 & 2 & 3 \\
\end{array} \]
FB 0 and FB 1 can simultaneously process fragments from rast 1
(Notice updates to frame buffer)
Extending to parallel geometry units
Starting state: commands enqueued

Input:

- Draw T1 → 1 2 3 4
- Draw T2 → 1 2 3 4
- Draw T3 → 1 2 3 4
- Draw T4 → 1 2

Assume batch size is 2 for assignment to geom units and to rasterizers.
Distribute triangles to geom units round-robin (batches of 2)

Input:

Draw \(\triangle T_1\) → 1 2 3 4

Draw \(\triangle T_2\) → 1 2 3 4

Draw \(\triangle T_3\) → 1 2 3 4

Draw \(\triangle T_4\) → 1 2

Interleaved render target
Geom 0 and geom 1 process triangles in parallel
(Results after T1 processed are shown. Note big triangle T1 broken into multiple work items. [Eldridge et al.])
Geom 0 and geom 1 process triangles in parallel
(Triangles enqueued in rast input queues. Note big triangles broken into multiple work items. [Eldridge et al.])

Input:
- Draw T1 → 1 2 3 4
- Draw T2 → 1 2 3 4
- Draw T3 → 1 2 3 4
- Draw T4 → 1 2

Interleaved render target

0 1
1 0
Geom 0 broadcasts ‘next’ token to rasterizers

Input:

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<td></td>
<td>5</td>
<td>6</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

Interleaved render target
Rast 0 and rast 1 process triangles from geom 0 in parallel
(Shaded fragments enqueued in frame-buffer unit input queues)

Input:
- Draw \( \Delta T_1 \) → 1 2 3 4
- Draw \( \Delta T_2 \) → 5 6 7
- Draw \( \Delta T_3 \) → 1 2 3 4
- Draw \( \Delta T_4 \) → 1 2

Interleaved render target
Rast 0 broadcasts ‘next’ token to FB units (end of geom 0, rast 0)

Input:

Draw \( \uparrow \) \( T_1 \) \( \rightarrow \) 1 2 3 4

Draw \( \uparrow \) \( T_2 \) \( \rightarrow \) 1 2 3 4

Draw \( \uparrow \) \( T_3 \) \( \rightarrow \) 1 2 3 4

Draw \( \uparrow \) \( T_4 \) \( \rightarrow \) 1 2

Interleaved render target
Frame-buffer units process frags from (geom 0, rast 0) in parallel
(Notice updates to frame buffer)

Input:

Draw \( T_1 \) \rightarrow 1 2 3 4 5 6 7
Draw \( T_2 \) \rightarrow 1 2 3 4
Draw \( T_3 \) \rightarrow 1 2 3 4
Draw \( T_4 \) \rightarrow 1 2

Interleaved render target

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“End of rast 0” token reached by FB: FB units start processing input from rast 1 (fragments from geom 0, rast 1)

Input:

Draw T1 → 1 2 3 4
Draw T2 → 1 2 3 4
Draw T3 → 1 2 3 4
Draw T4 → 1 2

Interleaved render target
“End of geom 0” token reached by rast units: rast units start processing input from geom 1 (note “end of geom 0, rast 1” token sent to rast input queues)
Rast 0 processes triangles from geom 1
(Note Rast 1 has work to do, but cannot make progress because its output queues are full)
Rast 0 broadcasts “end of geom 1, rast 0” token to frame-buffer units

Input:

Draw \( \land \) 1 2 3 4

Draw \( \land \) 2 1 3 4

Draw \( \land \) 3 1 2 3 4

Draw \( \land \) 4 1 2

Interleaved render target
Frame-buffer units process frags from (geom 0, rast 1) in parallel
(Notice updates to frame buffer. Also notice rast 1 can now make progress since space has become available)
Switch token reached by FB: FB units start processing input from (geom 1, rast 0)

Input:

- Draw $\triangle T_1 \rightarrow 1 \ 2 \ 3 \ 4$
- Draw $\triangle T_2 \rightarrow 1 \ 2 \ 3 \ 4$
- Draw $\triangle T_3 \rightarrow 1 \ 2 \ 3 \ 4$
- Draw $\triangle T_4 \rightarrow 1 \ 2$

Interleaved render target
Frame-buffer units process frags from (geom 1, rast 0) in parallel
(Notice updates to frame buffer)

Input:

Draw \(\text{T1}\) \(\rightarrow\) \(1\) \(2\) \(3\) \(4\)

Draw \(\text{T2}\) \(\rightarrow\) \(1\) \(2\) \(3\) \(4\)

Draw \(\text{T3}\) \(\rightarrow\) \(1\) \(2\) \(3\) \(4\)

Draw \(\text{T4}\) \(\rightarrow\) \(1\) \(2\)

Frame-buffer units process frags from (geom 1, rast 0) in parallel (Notice updates to frame buffer)
Switch token reached by FB: FB units start processing input from (geom 1, rast 1)

Input:

Draw \( \triangle T_1 \) → 1 2 3 4

Draw \( \triangle T_2 \) → 1 2 3 4

Draw \( \triangle T_3 \) → 1 2 3 4

Draw \( \triangle T_4 \) → 1 2
Frame-buffer units process frags from (geom 1, rast 1) in parallel (Notice updates to frame buffer)

Input:

- Draw $\Delta T1$ → $1 \ 2 \ 3 \ 4$
- Draw $\Delta T2$ → $1 \ 2 \ 3 \ 4$
- Draw $\Delta T3$ → $1 \ 2 \ 3 \ 4$
- Draw $\Delta T4$ → $1 \ 2$

Frame-buffer units process frags from (geom 1, rast 1) in parallel (Notice updates to frame buffer)

Interleaved render target

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Parallel scheduling with data amplification
Geometry amplification

Consider examples of one-to-many stage behavior during geometry processing in the graphics pipeline:

- Clipping amplifies geometry (clipping can result in multiple output primitives)

- Tessellation: pipeline permits thousands of vertices to be generated from a single base primitive (challenging to maintain highly parallel execution)

- Primitive processing (“geometry shader”) outputs up to 1024 floats worth of vertices per input primitive
Thought experiment

Assume round-robin distribution of eight primitives to geometry pipelines, one rasterizer unit.
Consider case of large amplification when processing T1

Result: one geometry unit (the one producing outputs from T1) is feeding the entire downstream pipeline
- Serialization of geometry processing: other geometry units are stalled because their output queues are full (they cannot be drained until all work from T1 is completed)
- Underutilization of rest of chip: unlikely that one geometry producer is fast enough to produce pipeline work at a rate that fills resources of rest of GPU.

Notice: output from T1 processing fills output queue
Thought experiment: design a scheduling strategy for this case

1. Design a solution that is performant when the expected amount of data amplification is low?
2. Design a solution that is performant when the expected amount of data amplification is high.
3. What about a solution that works well for both?

The ideal solution always executes with maximum parallelism (no stalls), and with maximal locality (units read and write to fixed size, on-chip inter-stage buffers), and (of course) preserves order.
Implementation 1: fixed on-chip storage

Approach 1: make on-chip buffers big enough to handle common cases, but tolerate stalls
- Run fast for low amplification (never move output queue data off chip)
- Run very slow under high amplification (serialization of processing due to blocked units). Bad performance cliff.
Implementation 2: worst-case allocation

Approach 2: never block geometry unit: allocate worst-case space in off-chip buffers (stored in DRAM)
- Run slower for low amplification (data goes off chip then read back in by rasterizers)
- No performance cliff for high amplification (still maximum parallelism, data still goes off chip)
- What is overall worst-case buffer allocation if the four geometry units above are Direct3D 11 geometry shaders?
Implementation 3: hybrid

Hybrid approach: allocate output buffers on chip, but spill to off-chip, worst-case size buffers under high amplification
- Run fast for low amplification (high parallelism, no memory traffic)
- Less of performance cliff for high amplification (high parallelism, but incurs more memory traffic)
NVIDIA GPU implementation

Optionally resort work after Hull shader (since amplification factor known)